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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/816,776   | 04/02/2004  | Amitabh Jain         | TI-34913A           | 2773             |
| 23494  | 7590        | 10/13/2004           | EXAMINER            |                  |
| TEXAS INSTRUMENTS INCORPORATED<br>P O BOX 655474, M/S 3999<br>DALLAS, TX 75265 |             |                      | BLUM, DAVID S       |                  |
|  |             |                      | ART UNIT            | PAPER NUMBER     |
|  |             |                      | 2813                |                  |

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/816,776

**Applicant(s)**

JAIN ET AL

**Examiner**

David S Blum

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

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This action is in response to the application filed 4/2/04.

## **DETAILED ACTION**

### ***Double Patenting***

1. Claim 17 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 16. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Mayur (US2003/0040130A1).

Mayur teaches all of the positive steps of claims 1-18.

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Regarding claim 1, mayor teaches providing a semiconductor (paragraph 0042), implanting a dopant species into the semiconductor (paragraph 0054) and annealing the implanted semiconductor at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1026 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

Regarding claim 2, the implant is amorphizing (paragraph 0054).

Regarding claim 3, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 4, the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, less than 100 nanoseconds (0.0001 milliseconds)).

Regarding claim 5, Mayur teaches providing a semiconductor (paragraph 0042), a patterned photoresist layer (paragraph 0051), implanting a dopant species into semiconductor (paragraph 0054), removing the photoresist (figure 2C shows patterned photoresist removed), and annealing with a solid phase epitaxy anneal (paragraph 0043, epitaxial, paragraph 0084, solid phase and paragraph 0047, conventional anneal). Although Mayur does not recite "solid phase epitaxy anneal, this is inferred from the process (same as the instant application) and that it is a solid phase anneal

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resulting in an epitaxial layer.) The anneal is at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1026 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

Regarding claim 6, the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, less than 100 nanoseconds (0.0001 milliseconds).

Regarding claim 7, the implant is amorphizing (paragraph 0054).

Regarding claim 8, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 9, Mayur teaches providing a semiconductor substrate (paragraph 0042), a gate dielectric layer (insulator 208), a gate electrode (210) on the gate dielectric, implanting dopant species into the semiconductor adjacent the gate electrodes (paragraph 0053), annealing the implanted semiconductor with solid phase epitaxy anneal between 550 and 950 C (paragraph 0047, diffusing dopants between 800-1100 C), and annealing at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1026 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

Regarding claim 10, the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, less than 100 nanoseconds (0.0001 milliseconds)).

Regarding claim 11, the amorphizing implant is preformed prior to the dopant implant (paragraph 0054).

Regarding claim 12, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 13, Mayur teaches forming a MOSFET transistor (paragraph 0006), providing a semiconductor substrate (paragraph 0042), a gate dielectric layer (insulator 208), a gate electrode (210) on the gate dielectric, implanting dopant species into the semiconductor adjacent the gate electrodes (paragraph 0053), implanting with gate sidewalls (as shown in figure 2F), annealing the implanted semiconductor with solid phase epitaxy anneal between 550 and 950 C (paragraph 0047, diffusing dopants between 800-1100 C), and annealing at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1026 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C)).

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Regarding claim 14, the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, less than 100 nanoseconds (0.0001 milliseconds)).

Regarding claim 15, the amorphizing implant is preformed prior to the first dopant implant (paragraph 0054).

Regarding claims 16 and 17, the amorphizing implant (amorphous implant) is preformed prior to the second dopant implant (paragraph 0054, amorphizing implant performed prior to well implant and source/drain implant, two different species).

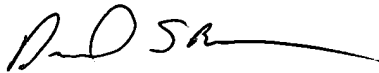
Regarding claim 18, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is [David.blum@USPTO.gov](mailto:David.blum@USPTO.gov) .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read "D. S. Blum", with a long horizontal flourish extending to the right.

David S. Blum

October 12, 2004